Absolute Maximum Ratings

Supply voltage range, V_{DD} ..... 0 V to 6.0 V
Input voltage range ..... -0.1V to VDD+0.1V
Operating free-air temperature range ..... -10°C to 85°C
Storage temperature range ..... -20°C to 125°C
Maximum reflow temperature ..... 260°C

Electrical Characteristics

Parameter	Condition	MIN	TYP	MAX	Units
V_{OUT} output impedance			10		kΩ
V_{OUT} settling time			1		µs
V_{OUT} maximum swing	2.5x gain		V_{DD}-0.3		V
V_{OUT} at dark	no light	0.60	0.84	1.1	V
V_{SAT}	15.6µm pitch		1.95		V
Linearity error per pixel	1x gain, V_{OUT}=5%-70% full-well	0.5	1	5	% error
Image lag	Clock setup-time	0.1	0.3	3.0	% V_{SAT}

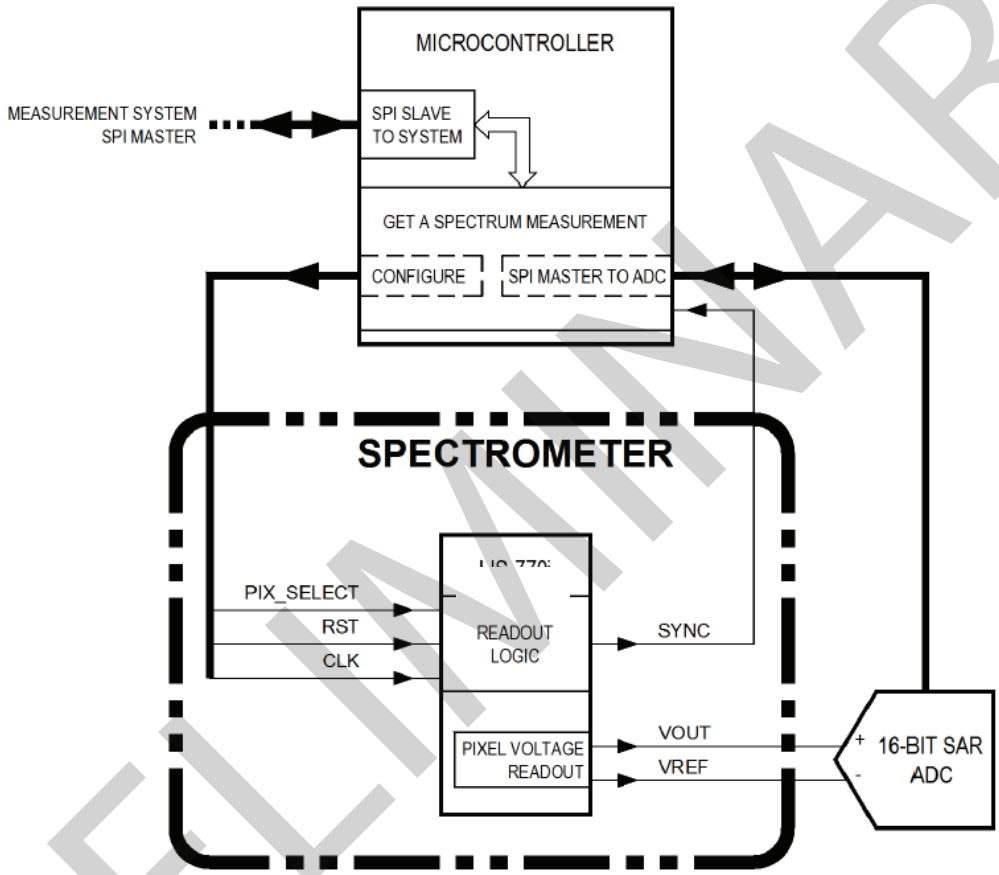
Recommended Operating Conditions

Symbol	Parameter	MIN	TYP	MAX	Units
V_{DD}	Supply voltage	2.8	3.0	3.3	V
	Power consumption while active		5.0	10	mW
	Power consumption in low-power mode		30		µW
$V_{in,HIGH}$	Input logic-level *HIGH*	V_{DD}-0.7		V_{DD}	V
$V_{in,LOW}$	Input logic-level *LOW*			0.7	V
f_{CLK}	Clock frequency	15	50	200	kHz
CLK_{HOLD}	Clock hold-time		10		ns
CLK_{SETUP}	Clock setup-time		10		ns

The spectrometer samples inputs on the rising edges of CLK. CLK_{HOLD} is the minimum time after a falling edge of CLK before RST is allowed to change value. CLK_{SETUP} is the minimum time RST must be stable before a rising edge of CLK to guarantee its value is sampled on the rising edge.

Spectrometer Interface

External hardware is required to interface the spectrometer and acquire a spectrum. The block diagram below shows the signals required to initalize, configure, and acquire a spectrum.



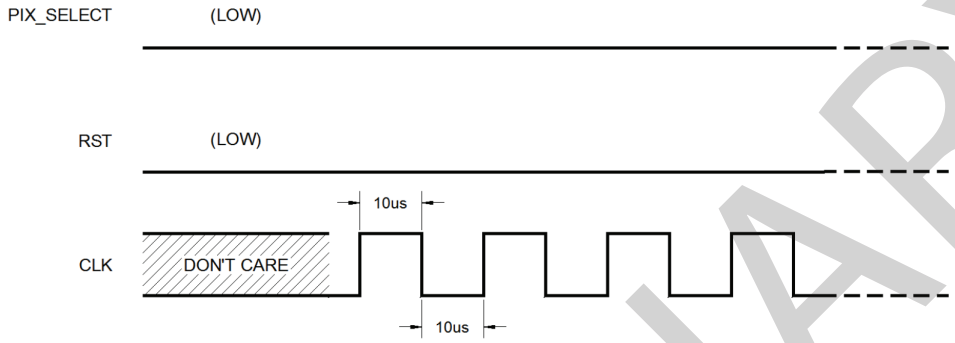
CLK, RST, and PIX_SELECT are logic-level inputs. The following timing diagrams show the logic level sequences for power-on initialization, spectrometer configuration, and spectrum acquisition. The spectrometer's linear array does *not* have a known default configuration on power-up; the initialization and configuration sequences must be run each time the device is powered up.

The choice of clock speed is determined by the ADC conversion settling time and the speed of communication with the ADC. 50kHz (shown in the timing diagrams) is slow enough for a 16-bit SAR to convert pixel voltages and to read out the converted digital value.

Chromation recommends dark-correcting the analog output before input to the ADC. Voltage reference selection depends on application-specific design considerations; Chromation recommends selecting an ADC voltage reference between 70% and 100% of V_{SAT}.

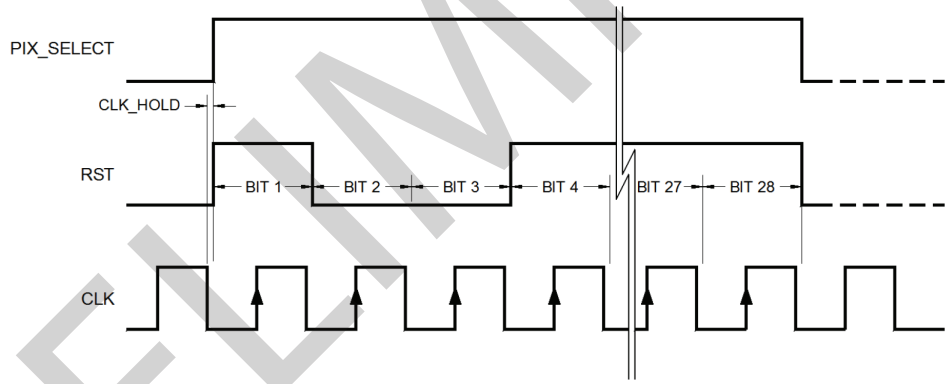
Initialization sequence after power-on

Start CLK after PIX_SELECT and RST are driven low.



Configuration sequence

The configuration sequence consists of shifting in 28 bits. Bits are shifted on the rising edge of CLK. The sequence starts with bit 1 and ends with bit 28.

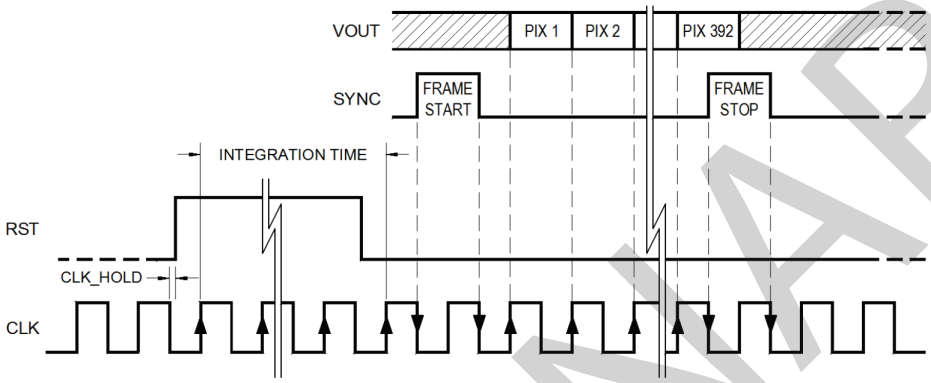


Bits 2 and 3 set analog gain. The programming sequence shown is for 1x gain. The table below shows the available gain configurations.

Gain Setting	Bit 2	Bit 3
1x	LOW	LOW
2.5x	LOW	HIGH
4x	HIGH	LOW
5x	HIGH	HIGH

Spectrum acquisition sequence

The spectrometer's linear array requires external logic level signals to execute spectrometer exposure and readout.



Integration time is set by holding RST high for the desired number of clock cycles. Exposure starts when HIGH on RST is sampled on the rising edge of CLK, and ends when LOW on RST is sampled on the rising edge of CLK. For example, a 10ms integration time can be achieved with a 50kHz CLK by holding RST high for 500 clock cycles.

After RST is driven LOW, SYNC goes high on the next falling edge of CLK and remains high for one clock cycle. Pixel readout begins on the next rising edge of CLK after SYNC goes low. During the last pixel readout SYNC goes high on the falling edge of CLK and remains high for one clock cycle.

During pixel readout each ADC converion should start on the rising edge of CLK and complete before the falling edge of CLK.

Pin Assignments

Pin Assignment:
10 VREF
12 VIDEO
13 GND
15 VDD
16 SYNC
17 PIX_SELECT
18 RST
20 CLK